REMARKS

In the Decision on Appeal dated April 7, 2009, rejections of claims 1-21 under § 112, second paragraph, were vacated; rejections of claims 1-7 and 16-21 based on Joffe and Mathur were affirmed; and rejections of claims 8-15 based on Mathur under § 102(b) were vacated. But the Board then rejected claims 8-15 by issuing a new ground of rejection under § 103(a) in light of Mathur. This present amendment is being filed pursuant 37 CFR 41.50(b)(1) which provides that the Appellant may reopen a prosecution before the Examiner when the Board issues a Decision on Appeal with new grounds of rejection. The amendments and remarks herein pertain only to claims 8-15 which were newly-rejected in the April 7, 2009 Decision on Appeal. Reconsideration of the application is respectfully requested.

It is noted herein that 37 CFR 41.50(b)(1) does not require a Request for Continued Examination (RCE) to accompany this present amendment in order to place the application back into prosecution, and so an RCE and the corresponding RCE fee are not included herewith.

Claims 8-15 have been amended. No new matter is added. Support for amendments to claim 8, for example, can be found throughout the specification and claims, such as for example in Figure 2B and the accompanying text in the Detailed Description.

REJECTIONS OF CLAIMS 8-15 UNDER 35 U.S.C. § 103

On page 22 of the Decision on Appeal, the Board vacated the Examiner's rejections of claims 8-15 under § 102(b) and newly rejected claims 8-15 under § 103(a) in view of Mathur standing alone.

The Board did not particularly address whether Mathur anticipated the buffer recited in the previous version of claim 8. On page 5 of the non-final Office Action mailed October 20, 2006, the Examiner found that the Mathur Abstract disclosed the buffer as recited in claim 1. (The Examiner later incorporated his findings with regards to claim 1 into his rejection of previous claim 8.)

The Mathur Abstract reads in part:

> A store-and-forward network switch uses an embedded dynamic-random-access memory (DRAM) packet memory. An input port controller receiving a packet writes the packet to the embedded packet memory. ... Packets are stored at row boundaries so that DRAM page-mode cycles predominate. Only one packet is written to each DRAM row or page.

Mathur fails to teach at least "a buffer associated with one of the plurality of ports and configured to assemble a stream of data words, as received by the one of the plurality of ports, into a single word having a predetermined width, wherein the predetermined width includes x number of bits, and *wherein y divided by x results in an integer greater than one*" as recited in amended claim 8 presented herein. The Mathur abstract states that a single packet is saved into a row line, but says nothing of the relation between the number of bits in the row line and the number of bits in the packet size (e.g., the relationship between x and y of amended claim 8). In fact, packets as used in Mathur are often of variable size, while memory bank rows as used in Mathur are a fixed size. Mathur could therefore not teach any consistent relationship between the size of the words written to memory and the size of the memory itself. Thus, Mathur fails to teach at least this quoted subject matter of amended claim 8.

Furthermore, Mathur's purpose in storing only a single packet per row is to have page-mode cycles predominate the DRAM access. Modifying the Mathur buffer to achieve the buffer of amended claim 8 would have not helped achieve this purpose. Also, because Mathur never writes more than one packet to a row, modifying Mathur to include the buffer of claim 8 – which in one embodiment covered by claim 8 restricts the size of words written to the memory to be at least half the size of the row – would result in much unused memory in Mathur's modified buffer. Thus, modifying Mathur to achieve the buffer of amended claim 8 would not only have been unhelpful in achieving Mathur's purpose, it would have also resulted in a more inefficient use of memory. It is therefore submitted that one of ordinary skill would have found no suggestion to modify Mathur to incorporate the buffer of claim 8.

For at least these reasons it is submitted that Mathur neither teaches nor suggests the buffer of claim 8. Thus, it is submitted that claim 8 is non-obvious and therefore patentable under § 103(a) in light of Mathur standing alone. Claims 9-15 depend from claim 8. For at

least the same reasons, it is therefore submitted that claims 9-15 are also patentable over Mathur standing alone.

CONCLUSION

It is submitted that claims 8-15 are in a condition for allowance. Accordingly, a Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present paper, the Examiner is kindly requested to contact the undersigned at (206) 407-1542. If any fees are due in connection with filing this paper, the Commissioner is authorized to charge the Deposit Account of Schwabe, Williamson and Wyatt, P.C., No. 50-0393.

Respectfully submitted,
SCHWABE, WILLIAMSON & WYATT, P.C.

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by: /Richard B. Leggett/
Richard B. Leggett
Reg. No.: 59,485

Schwabe, Williamson & Wyatt, P.C.
U.S. Bank Centre
1420 5th Avenue, Suite 3010
Seattle, Washington 98101
Telephone: 206-622-1711